

## 65V N-Ch Power MOSFET

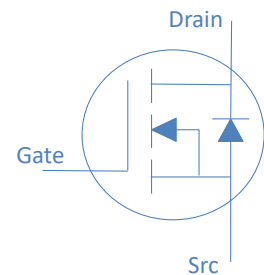
### Feature

- ◇ High Speed Power Switching, Logic level
- ◇ Enhanced Body diode dv/dt capability
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free, Halogen Free

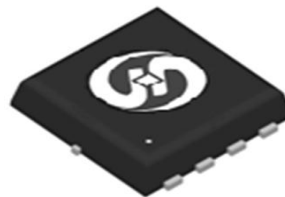
$V_{DS}$		65	V
$R_{DS(on),typ}$	$V_{GS}=10V$	7.5	m $\Omega$
$R_{DS(on),typ}$	$V_{GS}=4.5V$	10.5	m $\Omega$
$I_D$ (Silicon Limited)		39	A
$I_D$ (Package Limited)		36	A

### Application

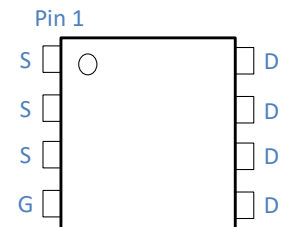
- ◇ Synchronous Rectification in SMPS
- ◇ Hard Switching and High Speed Circuit
- ◇ DC/DC in Telecoms and Industrial



DFN3.3x3.3



Part Number	Package	Marking
HGM090NE6AL	DFN 3.3x3.3	GM090NE6AL



### Absolute Maximum Ratings at $T_j=25^{\circ}C$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	$I_D$	$T_C=25^{\circ}C$	39	A
		$T_C=100^{\circ}C$	25	
		$T_C=25^{\circ}C$	36	
Continuous Drain Current (Package Limited)		$T_C=25^{\circ}C$	36	
Drain to Source Voltage	$V_{DS}$	-	65	V
Gate to Source Voltage	$V_{GS}$	-	$\pm 20$	V
Pulsed Drain Current	$I_{DM}$	-	250	A
Avalanche Energy, Single Pulse	$E_{AS}$	$L=0.4mH, T_C=25^{\circ}C$	45	mJ
Power Dissipation	$P_D$	$T_C=25^{\circ}C$	25	W
Operating and Storage Temperature	$T_J, T_{stg}$	-	-55 to 150	$^{\circ}C$

### Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	55	$^{\circ}C/W$
Thermal Resistance Junction-Case	$R_{\theta JC}$	5	$^{\circ}C/W$

**Electrical Characteristics at  $T_j=25^\circ\text{C}$  (unless otherwise specified)**
**Static Characteristics**

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	65	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.6	2.4	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS}=0V, V_{DS}=60V, T_j=25^\circ\text{C}$	-	-	1	$\mu A$
		$V_{GS}=0V, V_{DS}=60V, T_j=100^\circ\text{C}$	-	-	100	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$	-	7.5	9	$m\Omega$
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=5A$	-	10.5	13	$m\Omega$
Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=10A$	-	29	-	S
Gate Resistance	$R_G$	$V_{GS}=0V, V_{DS}$ Open, $f=1\text{MHz}$	-	1.4	-	$\Omega$

**Dynamic Characteristics**

Input Capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=30V, f=1\text{MHz}$	-	1170	-	pF
Output Capacitance	$C_{oss}$		-	518	-	
Reverse Transfer Capacitance	$C_{rss}$		-	31	-	
Total Gate Charge	$Q_g(10V)$	$V_{DD}=30V, I_D=10A, V_{GS}=10V$	-	20.5	-	nC
Total Gate Charge	$Q_g(4.5V)$		-	10.5	-	
Gate to Source Charge	$Q_{gs}$		-	2.5	-	
Gate to Drain (Miller) Charge	$Q_{gd}$		-	5.5	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=10A, V_{GS}=10V,$ $R_G=10\Omega,$	-	7	-	ns
Rise time	$t_r$		-	4	-	
Turn off Delay Time	$t_{d(off)}$		-	22	-	
Fall Time	$t_f$		-	5	-	

**Reverse Diode Characteristics**

Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_F=20A$	-	0.9	1.2	V
Reverse Recovery Time	$t_{rr}$	$V_R=30V, I_F=10A, dI_F/dt=100A/\mu s$	-	33	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	24	-	nC

Fig 1. Typical Output Characteristics

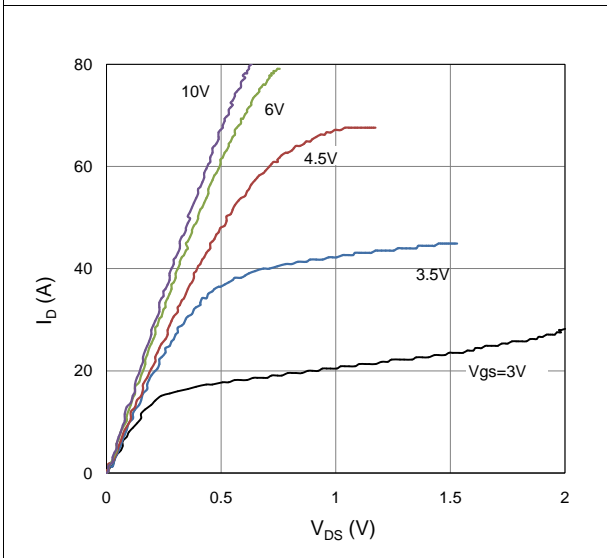


Figure 2. On-Resistance vs. Gate-Source Voltage

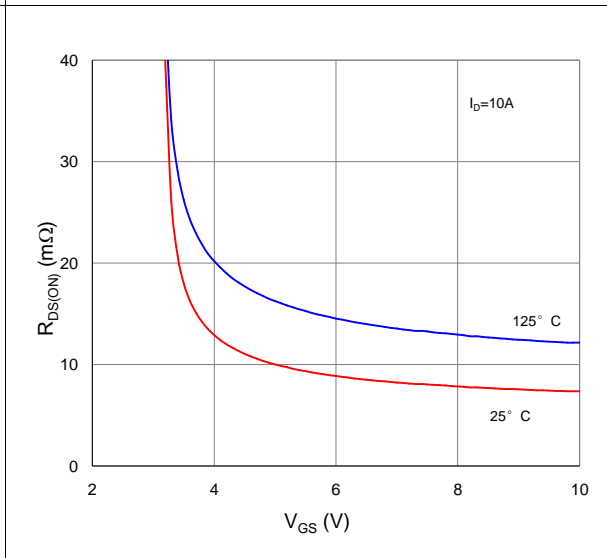


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

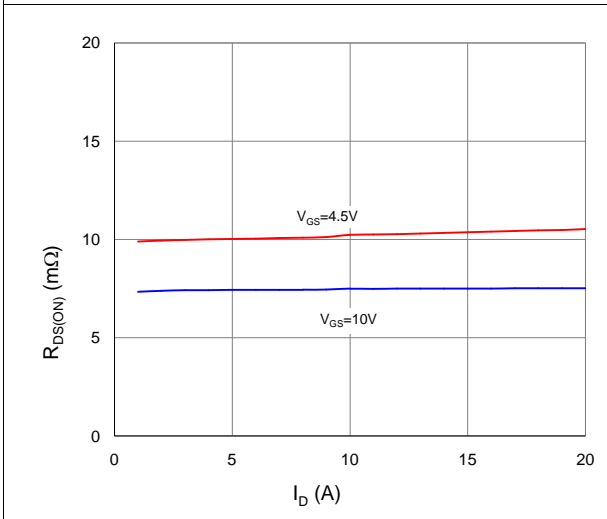


Figure 4. Normalized On-Resistance vs. Junction Temperature

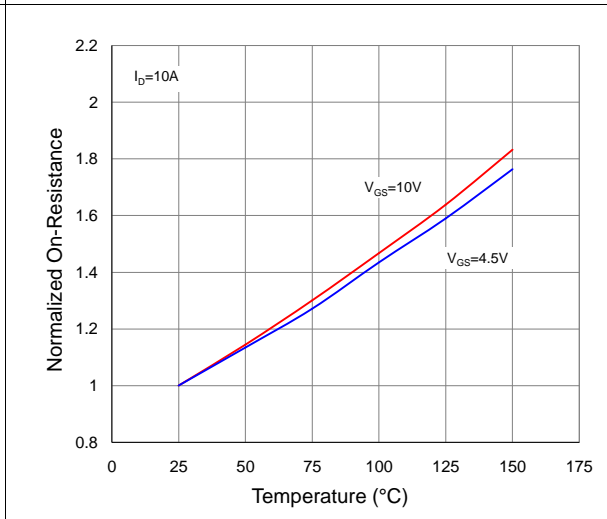


Figure 5. Typical Transfer Characteristics

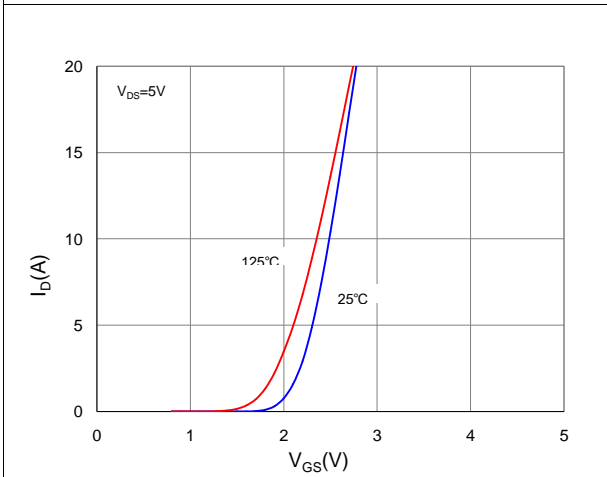


Figure 6. Typical Source-Drain Diode Forward Voltage

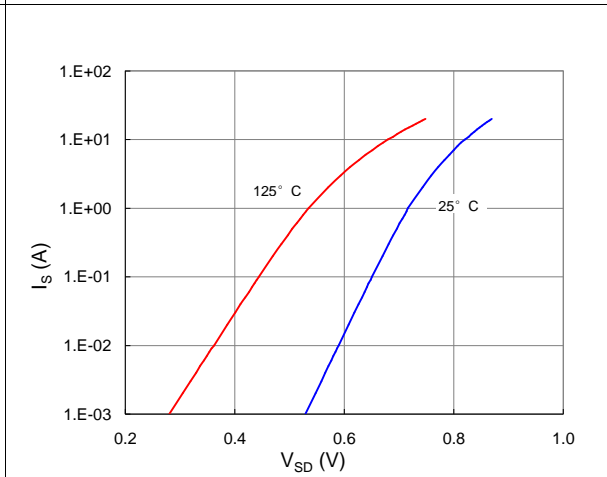


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

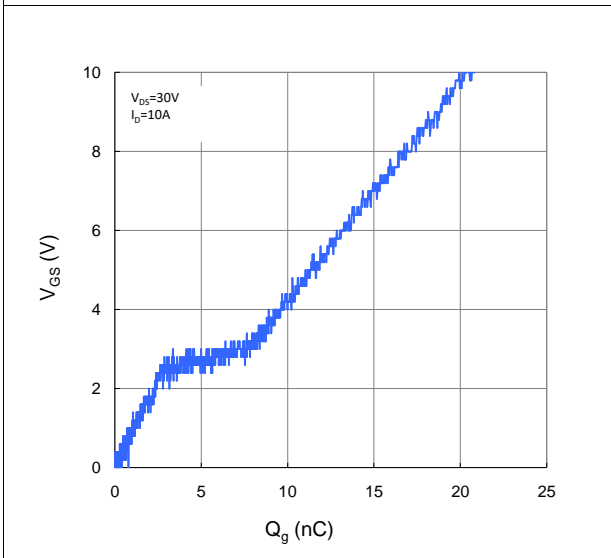


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

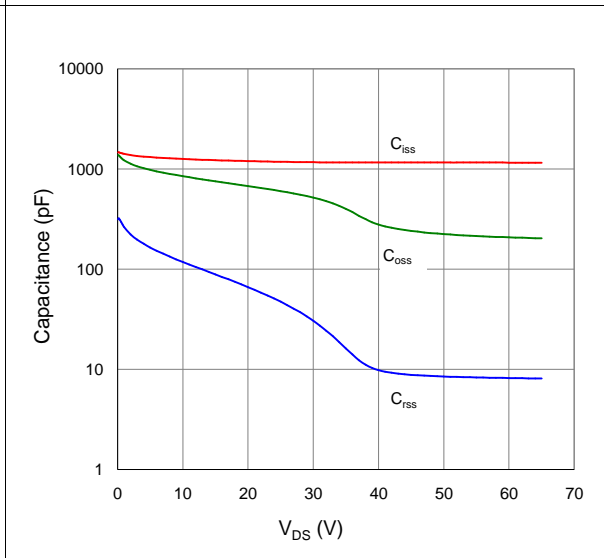


Figure 9. Maximum Safe Operating Area

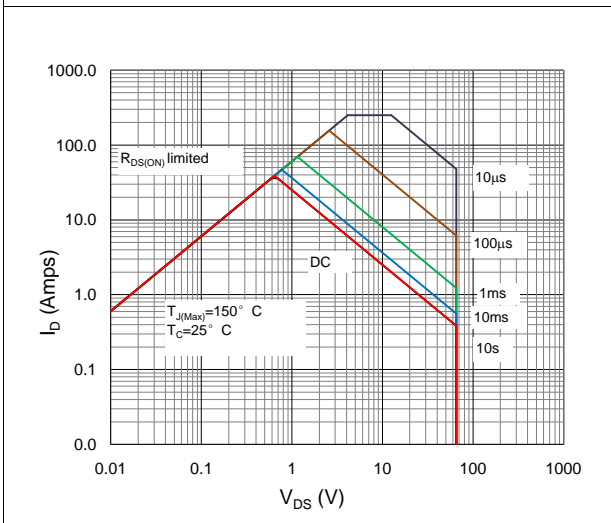


Figure 10. Maximum Drain Current vs. Case Temperature

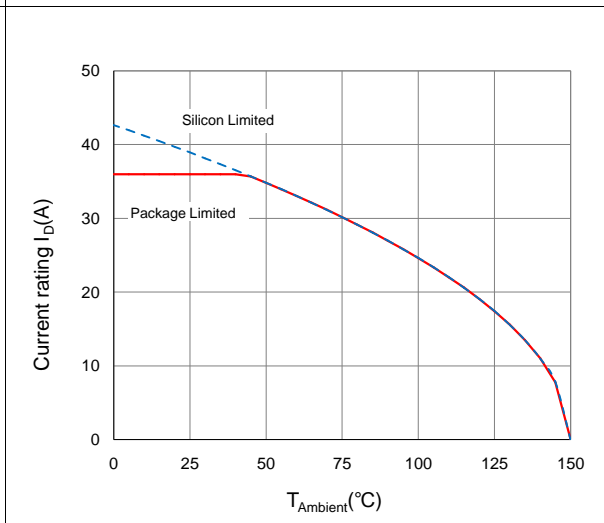
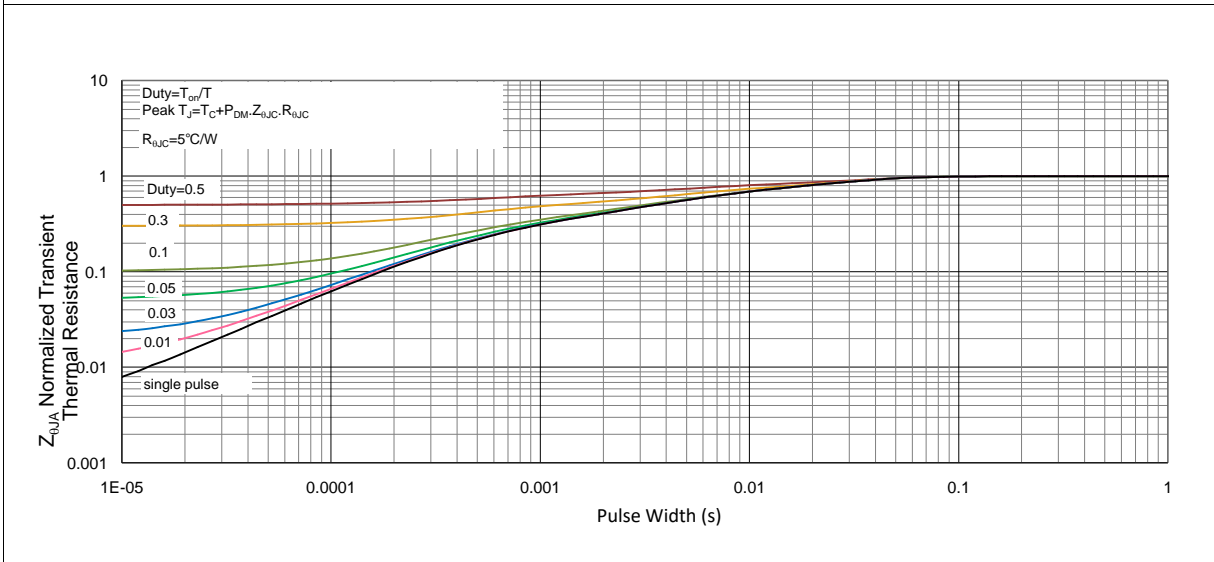
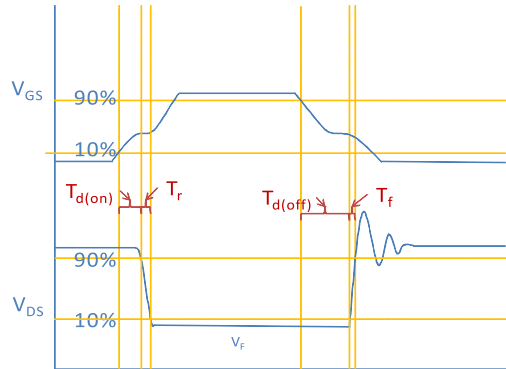
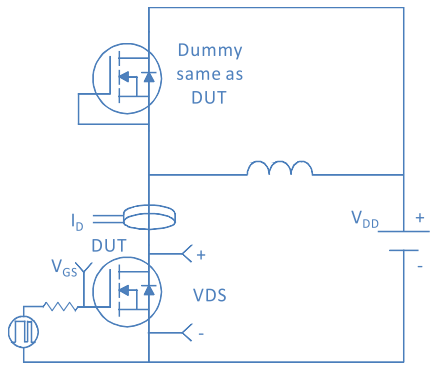


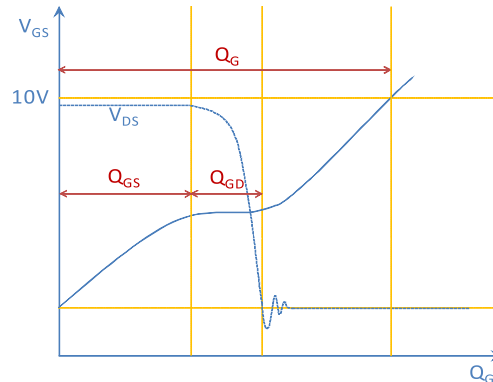
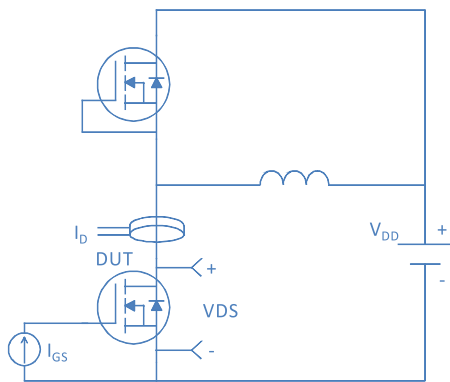
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



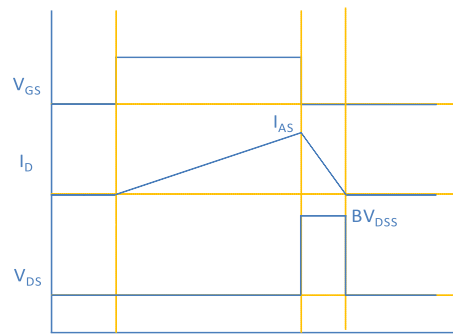
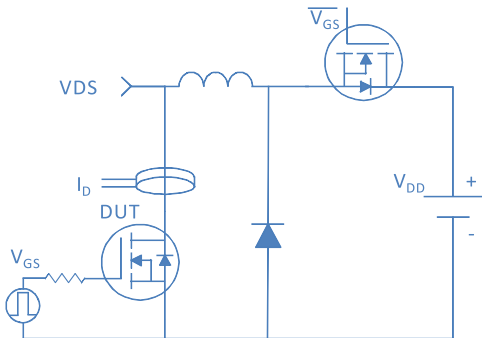
Inductive switching Test



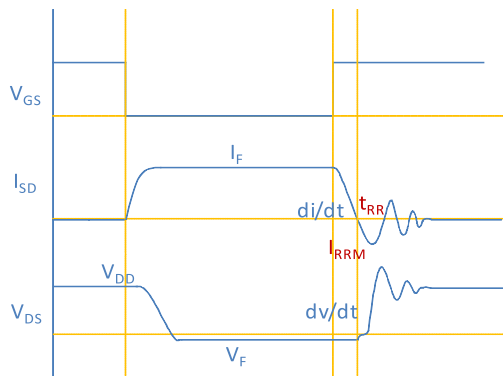
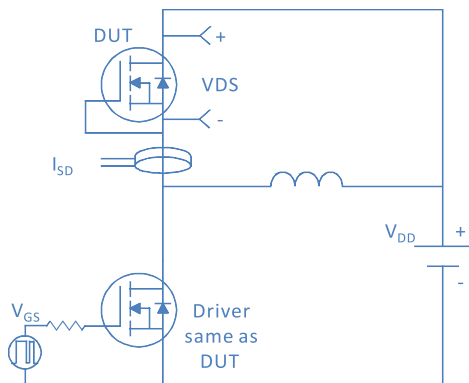
Gate Charge Test



Uclamped Inductive Switching (UIS) Test

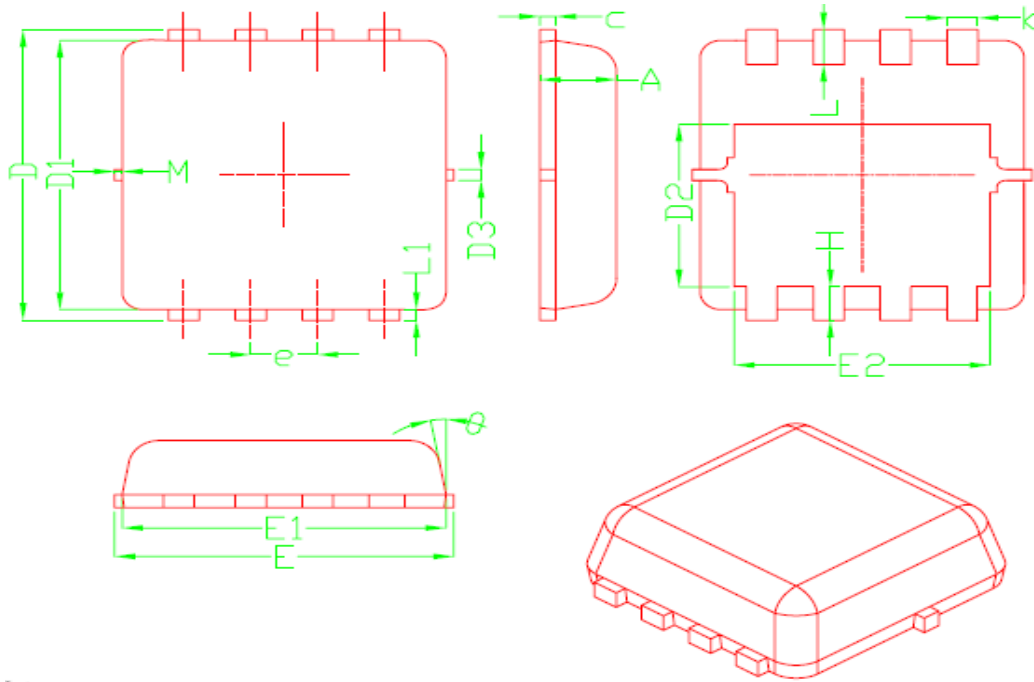


Diode Recovery Test



Package Outline

DFN3.3\*3.3\_P, 8 Leads



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
theta	---	10°	12°
M	*	*	0.15

\* Not specified